400G QSFP-DD DCO DWDMTunable Coherent 120km DOM Transceiver

QDD-ZR-400G

Applications

- Data Center Interconnect
- Metro/Edge Networks

Features

- Digital Coherent Optics module, QSFP-DD form factor, Type 2A
- IEEE 400GE or 4×100GE Ethernet compliant host interface
- Dispersion limited transmission reach up to 120km
- Coherent 400G optical interface based on OIF 400ZR implementation agreement
- Loss limited transmission reach up to 40km
- Full C-band tunable, 75GHz or 100GHz grid
- Case temperature range 0°C to 70°C
- Power dissipation < 18.5W

Description

The FS QSFP-DD Digital Coherent Optics (DCO) transceiver supports 400G coherent transmission for data center interconnect and metro/edge applications. The module is based on the OIF 400ZR implementation agreement [1], with an IEEE 400GE Ethernet compliant host interface [2] and a line interface using 59.8GBddual-polarization 16QAM modulation with Concatenated Forward Error Correction (C-FEC) code, supporting (amplified) DWDM transmission links up to 120km and loss limited (unamplified) reaches up to 40km. The module also supports multiplexing of 4× 100GE Ethernet signals [2] onto a 400G line interface.

The transceiver modules are compliant to the QSFP-DD MSA Hardware Specification [3], the Common Management Interface Specification (CMIS) [4] with extensions specified in the OIF Coherent CMIS implementation agreement [5]. The transceiver is RoHS compliant as described in Application Note AN-2038 [7-8].

Product Specifications

I. Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability. Application Note AN-2038 [7-8].

Parameter	Conditions		Symbol	Min.	Typ	Max	Unit	Note
DC Supply Voltage			V_{CC}	-0.3		3.6	V	
Low Speed I/O Voltages				-0.3		3.6	V	
Storage Temperature			T_S	-40	85	85	℃	
Case Operating Temperature			T_{OP}	-5	3.6	75	℃	
Relative Humidity	Non-condensing		RH	5	85	95	%	
Rx input Power			P_{Rxin}			18	dBm	
ESD Damage Threshold	Human body model (HBM)	DC pins		2000			V	
		RF pins		1000				

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

II. Environmental Specifications

Parameter	Conditions	Symbol	Min.	Typ	Max	Unit	Note
Storage Temperature		T_S	-40		85	℃	
Case Operating Temperature		T_{OP}	0		70	℃	
Relative Humidity	Non-condensing	RH	5		85	%	

III. Hostand Line Interface Modes

A. Host Interface Modes

Hos Interface ID [6]	Host Interface Description [6]	Modulation	Forward Error Correction Code	Nominal Symbol Rate (GBd)	Supported Line Interface IDs [6]
17	400GAUI-8	PAM4	RS(544,514)	26.5625	62, 63
13	4× 100GAUI-2	PAM4	RS(544,514)	26.5625	62, 63

B. Line Interface Modes

Hos Interface ID [6]	Line Interface Description [6]	Modulation	Forward Error Correction Code	Nominal Symbol Rate (GBd)	Spectral Shaping
62	400ZR, DWDM, Amplified	16QAM	C-FEC	59.8438	None
63	400ZR, Single Wavelength, Unamplified	16QAM	C-FEC	59.8438	None

IV. Electrical Characteristics

A. Power & Low Speed I/O

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Power Supply - General							
Power Supply Voltages	Including ripple, droop and noise below 100kHz		3.135	3.300	3.465	V	
Host RMS Noise Output	40Hz - 10MHz				25	mV	
Module RMS Noise Output	10Hz - 10MHz				30	mV	

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Power Supply - General							
Module Supply Noise Tolerance	10Hz - 10MHz, peak-to-peak	$PSNR_{mod}$			66	mV	
Module Inrush	Instantaneous peak duration	T_{ip}			50	μs	
	Initialization time	T_{init}			500	ms	
Power Supply - Low Power Mode							
Power Dissipation		P_{lp}			1.5	W	
Power Supply Current	Instantaneous peak current	$I_{CC,ip,lp}$			600	mA	
	Sustained peak current	$I_{CC,sp,lp}$			495		
	Steady state current	$I_{CC,lp}$			475		
Power Supply - High Power Mode - 400GE client							
Power Dissipation		P_{hp}			18.5	W	
Power Supply Current	Instantaneous peak current	$I_{CC,ip,hp}$			7.4	A	
	Sustained peak current	$I_{CC,sp,hp}$			6.2		
	Steady state current	$I_{CC,hp}$			6.0		
Power Supply - High Power Mode - 4× 100GE clients							
Power Dissipation		P_{hp}			19.5	W	
Power Supply Current	Instantaneous peak current	$I_{CC,ip,hp}$			7.8	A	
	Sustained peak current	$I_{CC,sp,hp}$			6.5		
	Steady state current	$I_{CC,hp}$			6.3		
Low Speed I/O							
Output Voltage, SCL and SDA	Output low	V_{OL}	0.0		0.4	V	
	Output high	V_{OH}	V_{CC}- 0.5		V_{CC}+ 0.3		
Input Voltage, SCL and SDA	Input low	V_{IL}	-0.3		0.3×V_{CC}	V	
	Input high	V_{IH}	0.7×V_{CC}		V_{CC}+0.5		
Capacitance for SCL and SDA I/O signal		Ci			14	pF	
Total Bus Capacitive Load for SCL and SDA	400kHz clock rate, 3.0kΩ pull-up, max.	Cb			100	pF	1
	400kHz clock rate, 1.6kΩ pull-up, max.				200		

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Low Speed I/O							
Input Voltage Current, InitMode, ResetL and ModSelL	Input voltage, low	V_{IL}	-0.3		0.8	V	
	Input voltage, high	V_{IH}	2.0		V_{CC}+0.3		
	Input current, 0V < V_{in} < V_{CC}	$\|I_{in}\|$			360	μA	
Output Voltage, IntL	Output low, I_{OL} = 2mA	V_{OL}	0.0		0.4	V	
	Output high, 10kΩ pull-up resistor to host V_{CC}	V_{OH}	V_{CC}-0.5		V_{CC}+0.3		
Output Voltage, ModPrsL	Output low, I_{OL} = 2mA	V_{OL}	0.0		0.4	V	2
	Output high	V_{OH}					

Notes:

1. For 1000kHz clock rate refer to Figure 6 in [3].
2. ModPrsL can be implemented as a short-circuit to GND on the module.

B. High Speed Data I/O

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Transmitter (Module Input) – 400GAUI-8, 100GAUI-2							
Signaling Rate Per Lane				Per IEEE Std 802.3 [2], Annex 120E, Table 120E-7		GBd	
Differential pk-pk Input Voltage Tolerance						mV	
Differential Input Return Loss						dB	
Differential to Common Mode Input Return Loss						dB	
Differential Termination Mismatch						%	
Module Stressed Input Test							
Single-ended Voltage Tolerance Range						V	
DC Common Mode Voltage						mV	
Receiver (Module Output) – 400GAUI-8, 100GAUI-2							
Signaling Rate Per Lane				Per IEEE Std 802.3 [2], Annex 120E, Table 120E-3		GBd	
AC Common-Mode Output Voltage						mV	

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Receiver (Module Output) – 400GAUI-8, 100GAUI-2							
Differential Peak-to-Peak Output Voltage						mV	
Near-end ESMW						UI	
Near-end Eye Height, Differential						mV	
Far-end ESMW						UI	
Far-end Eye Height, Differential						mV	
Far-end Pre-cursor ISI Ratio				Per IEEE Std 802.3 [2], Annex 120E, Table 120E–3		%	
Differential Output Return Loss						dB	
Common to Differential Mode Conversion Return Loss						dB	
Differential Termination Mismatch						%	
Transition Time						ps	
DC Common Mode Voltage						mV	

V. Digital Diagnostic Functions

The FSQSFP-DD-DCO module supports the diagnostics interface specified in the Mechanical Specification with extensions specified in the OIF Coherent CMIS implementation agreement [5]. See also Coherent application note AN-2200.

VI.Pin Description

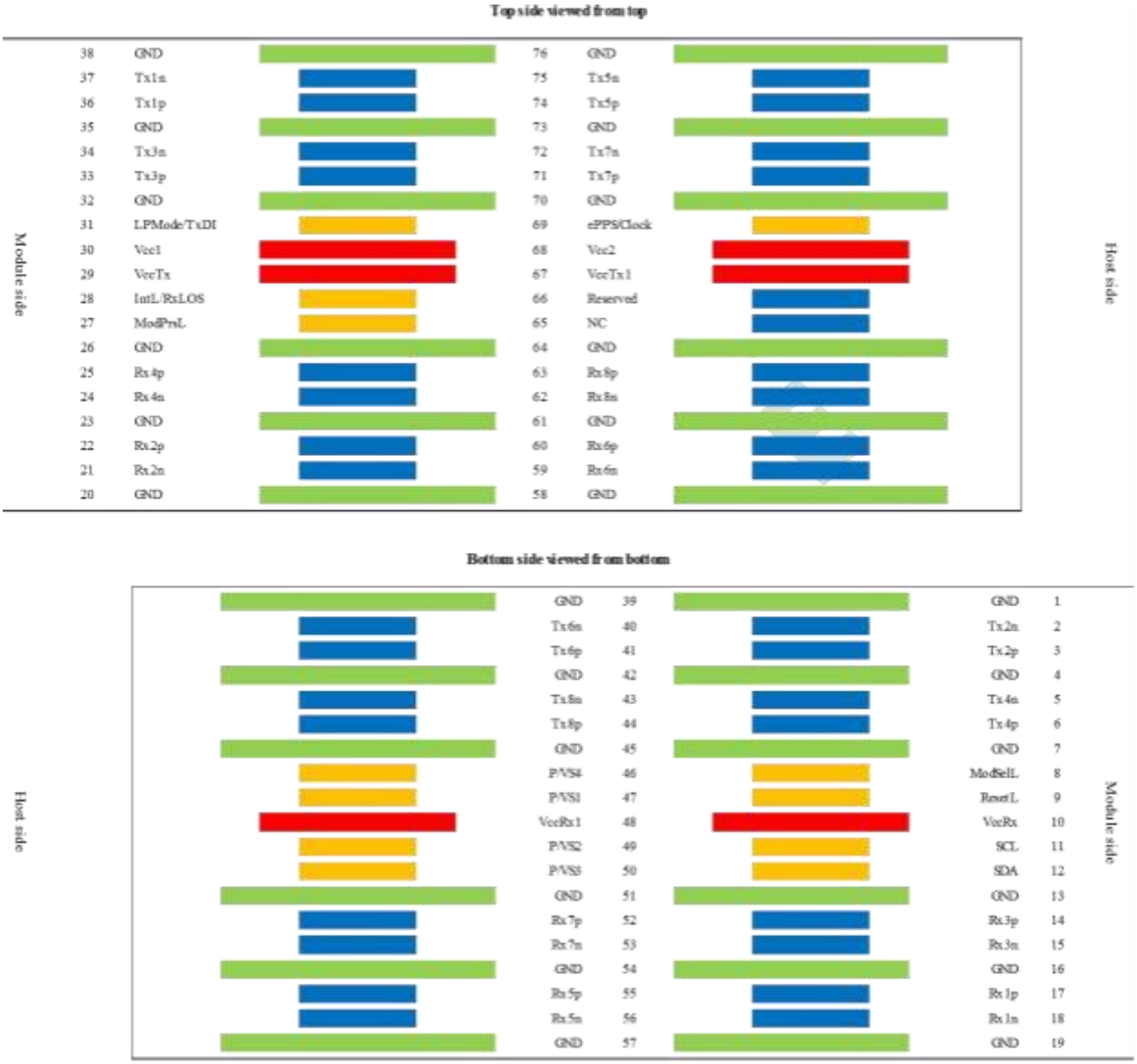


Figure 1 Module Pad Layout

VII. Pin Function Definitions

Pin	Logic	Symbol	Description	Plug Sequence[3]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter inverted data input	3B	
3	CML-I	Tx2p	Transmitter non-inverted data input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter inverted data input	3B	
6	CML-I	Tx4p	Transmitter non-inverted data input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module select	3B	
9	LVTTL-I	ResetL	Module reset	3B	
10		VccRx	+3.3V power supply receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver non-inverted data output	3B	
15	CML-O	Rx3n	Receiver inverted data output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver non-inverted data output	3B	
18	CML-O	Rx1n	Receiver inverted data output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver inverted data output	3B	
22	CML-O	Rx2p	Receiver non-inverted data output	3B	
23		GND	Ground	1B	1

Pin	Logic	Symbol	Description	Plug Sequence[3]	Notes
24	CML-O	Rx4n	Receiver inverted data output	3B	
25	CML-O	Rx4p	Receiver non-inverted data output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module present	3B	1
28	LVTTL-O	IntL/RxLOSL	Interrupt / Optional RxLOS	3B	
29		VccTx	+3.3V power supply transmitter	2B	2
30		Vcc1	+3.3V power supply	2B	2
31	LVTTL-I	LPMode/TxDIS	Low power mode / Optional Tx disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter non-inverted data input	3B	
34	CML-I	Tx3n	Transmitter inverted data input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter non-inverted data input	3B	
37	CML-I	Tx1n	Transmitter inverted data input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter inverted data input	3A	
41	CML-I	Tx6p	Transmitter non-inverted data input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter inverted data input	3A	
44	CML-I	Tx8p	Transmitter non-inverted data input	3A	
45		GND	Ground	1A	1
46	LVCMOS/CML-I	P/VS4	Programmable / Module vendor specific 4	3A	5

Pin	Logic	Symbol	Description	Plug Sequence[3]	Notes
47	LVCMOS/CML-I	P/VS1	Programmable / Module vendor specific 1	3A	5
48		VccRx1	+3.3V power supply	2A	2
49	LVCMOS/CML-O	P/VS2	Programmable / Module vendor specific 2	3A	5
50	LVCMOS/CML-O	P/VS3	Programmable / Module vendor specific 3	3A	5
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver non-inverted data output	3A	
53	CML-O	Rx7n	Receiver inverted data output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver non-inverted data output	3A	
56	CML-O	Rx5n	Receiver inverted data output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver inverted data output	3A	
60	CML-O	Rx6p	Receiver non-inverted data output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver inverted data output	3A	
63	CML-O	Rx8p	Receiver non-inverted data output	3A	
64		GND	Ground	1A	1
65		NC	No connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	+3.3V power supply	2A	2
68		Vcc2	+3.3V power supply	2A	2
69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input	3A	6

Pin	Logic	Symbol	Description	Plug Sequence[3]	Notes
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter non-inverted data input	3A	
72	CML-I	Tx7n	Transmitter inverted data input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter non-inverted data input	3A	
75	CML-I	Tx5n	Transmitter inverted data input	3A	
76		GND	Ground	1A	1

Note:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector GND contact is rated for a maximum current of 500 mA.

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Each connector Vcc contact is rated for a maximum current of 1500 mA.

3. Reserved and No Connect pads recommended to be terminated with 10 kΩ to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module.

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.

5. On new designs not used P/VSx signals are recommended to be terminated on the host with 10 kΩ .

6. ePPS/Clock if not used recommended to be terminated with 50 Ω to ground on the host.

VIII. Optical Characteristics

A. General

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Symbol Rate		Rbaud		59.84		GBd	
Modulation Format				16QAM			
Channel Frequency Range	100GHz grid	vC	191.400		196.100	THz	
	75GHz grid		191.375		196.100		
Channel Spacing	100GHz grid	ΔvC		100		GHz	
	75GHz grid			75			
Frequency Accuracy		δvC	-1.5		1.5	GHz	
Laser Intrinsic Linewidth	Calculated based on FM noise power spectral density (PSD) measurement	LW			300	kHz	
Side-mode Suppression Ratio	No modulation	SMSR	40			dB	
IRelative Intensity Noise	Peak over 0.2GHz < f < 10GHz	RIN			-140	dB/Hz	
	Average over 0.2GHz < f < 10GHz				-145		

B. Transmitter

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Tx Output Power Configurable Range		$P_{Tx,out}$	-13	0	-9	dBm	1
Tx Output Power Adjustment Resolution					0.1	dB	
Tx Output Power Tolerance		$\delta P_{Tx,out}$	-1.0		1.0	dB	2
Tx Output Power Monitor Range		$P_{Tx,m}$	-14		-8	dBm	
Tx Output Power Monitor Accuracy		$\delta P_{Tx,m}$	-1.0		1.0	dB	3
Tx Output Power During Tuning or When Tx Disabled		$P_{Tx,dark}$			-35	dBm	
Tx Output Power Imbalance Between X- and Y-polarizations		$\Delta P_{X/Y}$			1.5	dB	
Tx XY Skew					5.0	ps	

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Tx IQ Offset					-26	dB	
Tx IQ Imbalance					1.0	dB	
Tx Quadrature Error					5.0	°	
Tx IQ Skew					0.75	ps	
Tx In-band Optical Signal to Noise Ratio	Under modulation, $\|\Delta f\| < 150$ GHz	$OSNR_{in}$	39			dB/ 0.1nm	
Tx Out-of-band Optical Signal to Noise Ratio	Under modulation, $\|\Delta f\| > 150$ GHz	$OSNR_{out}$	30			dB/ 0.1nm	
Tx Reflectance					-27	dB	

Note:

1. Range of target Tx output power values for which other Tx specifications can be maintained.
2. Deviation from target value under closed loop control, over all operating conditions and life.
3. Tx optical output power monitor reading relative to actual Tx output power.

C. Receiver

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Rx Signal Input Power (amplified)	Full Rx OSNR tolerance	$P_{Rx,sig}$	-12		0	dBm	
	Extended range		-15		1		1
Rx OSNR Tolerance			26			dB/ 0.1nm	
CD Tolerance	OSNR penalty < 0.5dB		-2.4		2.4	ns/nm	2
PMD Tolerance	OSNR penalty < 0.5dB				10	ps	2
Tolerance to Change in SOP	OSNR penalty < 0.5dB				60	krad/s	2
Polarization Dependent Loss OSNR Penalty	1dB PDL				0.5	dB	2
	2dB PDL				1.0		
	4dB PDL				2.0		
Rx Signal Input Power Transient Amplitude	Peak excursion from steady state (within Rx signal input power range)		-3		3	dB	

Parameter	Conditions		Symbol	Min	Typ	Max	Unit	Notes
Rx Signal Input Power Transient Rise/Fall Time				0.1			ms	
Rx Signal Input Power (unamplified)	OSNR > 35dB/0.1nm			-20		0	dBm	
Rx Signal Input Power Monitor Range			$P_{Rx,m(s)}$	-22		1	dBm	
Rx Signal Input Power Monitor Accuracy			$\delta P_{Rx,m(s)}$	-2.0		2.0	dB	
Rx Total Input Power Monitor Range			$P_{Rx,m(t)}$	-22		3	dBm	
Rx Total Input Power Monitor Accuracy		-22dBm to -18dBm	$\delta P_{Rx,m(t)}$	–2.0		2.0	dB	
		-18dBm to +3dBm		-1.5		1.5		
Rx Reflectance							dB	

Note:

1. Rx signal input power range over which performance can be guaranteed with <1dB OSNR penalty relative to Rx OSNR tolerance limit.
2. Rx OSNR penalty is specified for Rx signal input powers <0dBm.

IX. Module Management Timing Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Optical							
Tx Turn on Time	Warm start				100	ms	
	Cold start				150	s	
Rx Acquisition Time	Warm start				30	ms	
	Cold start				150	s	
Tx/Rx Channel Tuning Time					30	s	
Soft Control and Status Functions							
MgmtInit Duration	Time from power on[1], hot plug or rising edge of reset until completion of the MgmtInit State				2000	ms	1
ResetL Assert Time	Minimum pulse time on the ResetL signal to initiate a module reset.		10			μs	

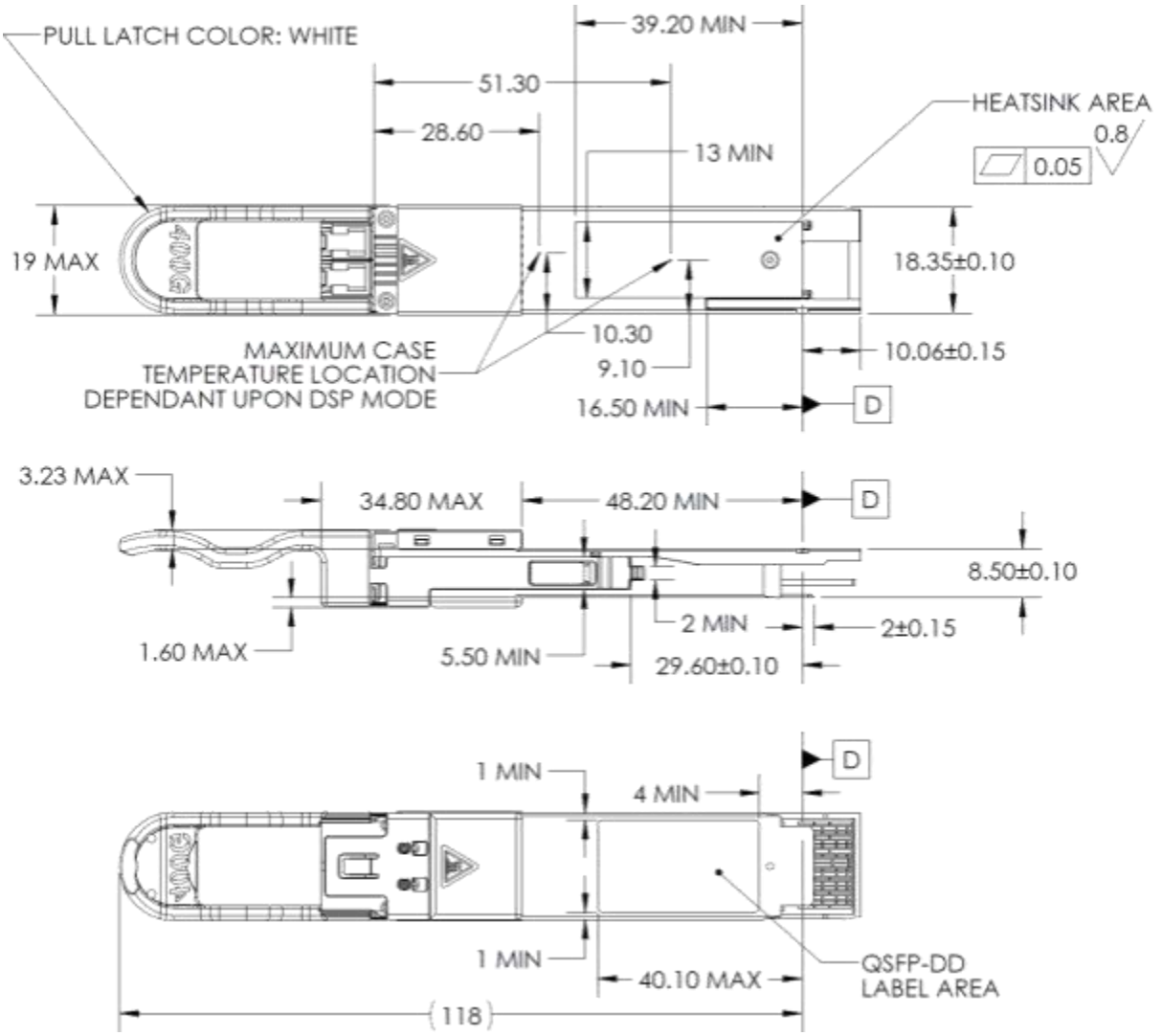
Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Soft Control and Status Functions							
IntL/RxLOS Mode Change Time	Time to change between IntL and RxLOSL modes ofthe dual-mode signal IntL/RxLOSL.				100	ms	
LPMode/TxDis Mode Change Time	Time to change between LPMode and TxDis modes ofthe LPMode/TxDis signal.				100	ms	
IntL Assert Time	Time from occurrence of condition triggering IntL until Vout:IntL=Vol				200	ms	
IntL Deassert Time	Time from clear on read[2] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.				500	μs	2
RxLOS Assert Time	Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted[3].				1	ms	3
RxLOS Deassert Time	Time from optical signal above the LOS deassert threshold to when the module releases the RxLOS signal to high.				3	ms	
Tx Disable Assert Time	Time from Tx Disable bit set (value = 1b)[4] until optical output falls below 10% of nominal				1	ms	4
Tx Disable Deassert Time	Time from Tx Disable bit cleared (value = 0b)[4] until optical output rises above 90% of nominal				100	ms	4
Tx Fault Assert Time	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.				200	ms	
Flag Assert Time	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.				200	ms	
Mask Assert Time	Time from mask bit set (value=1b)[5] until associated IntL assertion is inhibited.				100	ms	5
Mask Deassert Time	Time from mask bit cleared (value=0b)[5] until associated IntL operation resumes.				100	ms	5
Data Path Tx Turn On Max Duration[6]	Maximum duration of Tx Turn On state.		see CMIS memory 01h:168				6
Data Path Tx Turn Off Max Duration[6]	Maximum duration of Tx Turn Off state.		see CMIS memory 01h:168				6
Data Path Deinit Max Duration[6]	Maximum duration of Data Path DeInit state.		see CMIS memory 01h:144				6
Data Path Init Max Duration[6]	Maximum duration of Data Path Init state.		see CMIS memory 01h:144				6

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Soft Control and Status Functions							
Module Pwr Up Max Duration[7]	Maximum duration of Module Pwr Up state.			see CMIS memory 01h:167			7
Module Pwr Dn Max Duration[7]	Maximum duration of Module Pwr Dn state.			see CMIS memory 01h:167			7
I/O Timing for Squelch & Disable							
Rx Squelch Assert Time	Time from loss of Rx input signal until the squelched output condition is reached.				15	ms	
Rx Squelch Deassert Time	Time from resumption of Rx input signals until normal Rx output condition is reached.				50	ms	
Tx Squelch Assert Time	Time from loss ofTx input signal until the squelched output condition is reached.				400	ms	
Tx Squelch Deassert Time	Time from resumption of Tx input signal until the normal Tx output condition is reached.				1.5	s	
Rx Output Disable Assert Time	Time from Rx Output Disable bit set (value= 1b)[4] until Rx output falls below 10% of nominal				100	ms	4
Rx Output Disable Deassert Time	Time from Rx Output Disable bit cleared (value = 0b)[4] until Rx output rises above 90% of nominal				100	ms	4
Squelch Disable Assert Time	This applies to Rx and Tx Squelch and is the time from bit set (value = 1b)[4] until squelch functionality is disabled.				100	ms	4
Squelch Disable Deassert Time	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[4] until squelch functionality is enabled.				100	ms	4

Note:

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified.
2. Measured from low to high SDA edge of the Stop condition of the read transaction.
3. RxLOS condition is defined as (a) Rx input power below threshold or (b) DSP loss of signal.
4. Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction.
5. Measured from low to high SDA edge of the Stop condition of the write transaction.
6. Measured from the low to high SDA edge of the Stop condition of the Write transaction until the IntL for the state change Vout:IntL=Vol, unless the module advertises a less than 1 ms duration in which case there is no defined measurement.
7. Measured from the low to high SDA edge of the Stop condition of the Write transaction until the IntL for the state change Vout:IntL=Vol.

X. Mechanical Specifications



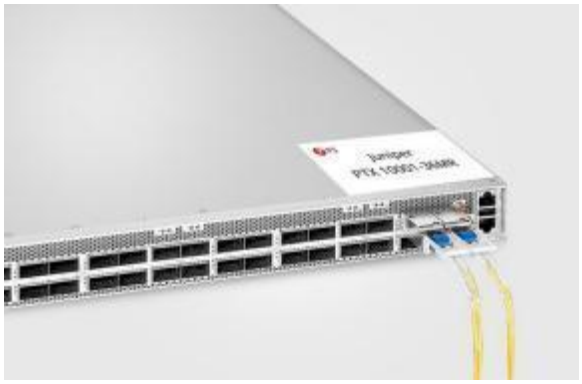
Test Center

I.CompatibilityTesting

Each fiber optical transceiver has been tested in host device on site in FS Assured Program to ensure full compatibility with over 200 vendors.

Cisco Nexus9000 C9316D-GX

Arista-DCS-7280DR3K-24-F



Juniper PTX10001-36MR

Juniper QFX 5220-32cd

Dell Z9332F-ON

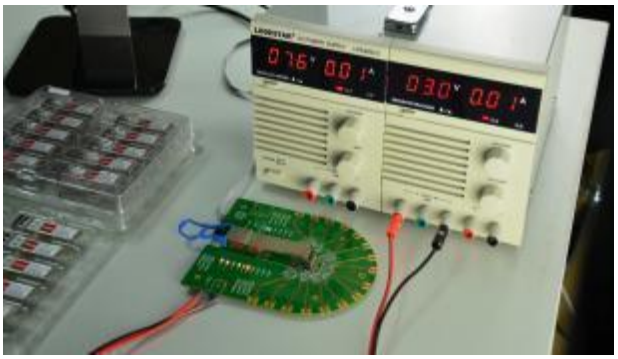
FS N9510-64D

Above is partofour testbed network equipment. For more information, please clickthe Test Bed PDF. Itwillbe updated in realtime as we expand our portfolio.

II. Test Assured Program

FS.COM truly understands the value of compatibility and interoperability to each optics. Every module FS.COM provides must run through programming and an extensive series of platform diagnostic tests to prove its performance and compatibility. In our test center, we care of every detail from staff to facilities-professionally trained staff, advanced test facilities and comprehensive original-brand switches, to ensure our customers to receive the optics with superior quality.

Our smart data system allows effective product management and quality control according to the unique serial number, properly tracing the order, shipment and every part.



Our in-house coding facility programs all of our parts to standard OEM specs for compatibility on all major vendors and systems such as Cisco, Juniper, Brocade, HP, Dell, Arista and so on.

With a comprehensive line of original-brand switches, we can recreate an environment and test each optics in practical application to ensure quality and distance.

The last test assured step to ensure our products to be shipped with perfect package.

Ordering Information

Part Number	Description
QDD-ZR-400G	400GQSFP-DD-DCO-DWDM Tunable Coherent 120km DOM Transceiver