

400G QSFP-DD DCO DWDMTunable Coherent 120km DOM Transceiver

QDD-ZRP-400G



Application

- Data Center Interconnect
- Metro/Edge Networks

Features

- Digital Coherent Optics module, QSFP-DD form factor, Type 2A
- IEEE 400GE or n×100GE (n = 1 ...4) Ethernet compliant host interface
- Coherent 400G/300G/200G/ 100G optical interface based on OpenZR+ MSA
- Transmission reach > 600km at 400G, with extended reaches at lower data rates
- Full C-band tunable with flexible grid support
- Case temperature range 0°C to 70°C
- Power dissipation < 22.5W

Description

The QSFP-DD Digital Coherent Optics (DCO) transceiver supports multi-rate coherent transmission for metro/regional and data center interconnect applications. On the host side, the module can accommodate either a single IEEE 400GE Ethernet signal or multiple 100GE Ethernet signals (n = 1...4) that are multiplexed onto a single line interface. On the line side the module supports 400G, 300G, or 200G line interfaces with 60GBd dual-polarization 16QAM, 8QAM, or QPSK modulation, respectively, as well as a 100G line interface with 30GBd dual-polarization QPSK modulation, as specified by the OpenZR+ MSA.

Product Specifications

I. Absolute Maximum Rating

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Conditions	Symbol	Min.	Typ	Max	Unit	Note
DC Supply Voltage		V _{CC}	-0.3		3.6	V	
Low Speed I/O Voltages			-0.3		3.6	V	
Storage Temperature		T _S	-40		85	°C	
Case Operating Temperature		T _{OP}	-5		75	°C	
Relative Humidity	Non-condensing	RH	5		95	%	
Rx Input Power		P _{Rxin}			18	dBm	
ESD Damage Threshold	Human body model (HBM)	DC pins		2000		V	
		RF pins		1000			

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

II. Environmental Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Note
Storage Temperature		T _s	-40		85	°C	
Case Operating Temperature		T _{OP}	0		70	°C	
Relative Humidity	Non-condensing	RH	5		85	%	

III. Hostand Line Interface Modes

A. Host Interface Modes

Hos Interface ID [7]	Host Interface Description [7]	Modulation	Forward Error Correction Code	Nominal Symbol Rate (GBd)	Supported Line Interface IDs [7]
17	400GAUI-8	PAM4	RS(544,514)	26.5625	70, 62
13	4× 100GAUI-2	PAM4	RS(544,514)	26.5625	70, 62
13	3× 100GAUI-2	PAM4	RS(544,514)	26.5625	71
13	2× 100GAUI-2	PAM4	RS(544,514)	26.5625	72
13	100GAUI-2	PAM4	RS(544,514)	26.5625	73

B. Line Interface Modes

Hos Interface ID [6]	Line Interface Description [6]	Modulation	Forward Error Correction Code	Nominal Symbol Rate (GBd)	Spectral Shaping
70	ZR400-OFEC-16QAM	16QAM	O-FEC	60.1385	None
71	ZR300-OFEC-8QAM	8QAM	O-FEC	60.1385	None
72	ZR200-OFEC-QPSK	QPSK	O-FEC	60.1385	None
73	ZR100-OFEC-QPSK	QPSK	O-FEC	30.0693	None
62	400ZR, DWDM, Amplified	16QAM	C-FEC	59.8438	None

IV. Electrical Characteristics

A. Power & Low Speed I/O

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Power Supply - General							
Power Supply Voltages	Including ripple, droop and noise below 100kHz		3.135	3.300	3.465	V	
Host RMS Noise Output	40Hz - 10MHz				25	mV	
Module RMS Noise Output	10Hz - 10MHz				30	mV	
Module Supply Noise Tolerance	10Hz - 10MHz, peak-to-peak	PSNR _{mod}			66	mV	
Module Inrush	Instantaneous peak duration	T _{ip}			50	μs	
	Initialization time	T _{init}			500	ms	
Power Supply - Low Power Mode							
Power Dissipation		P _p			1.5	W	
Power Supply Current	Instantaneous peak current	I _{CC,ip,lp}			600	mA	
	Sustained peak current	I _{CC,sp,lp}			495		
	Steady state current	I _{CC,lp}			475		
Power Supply - High Power Mode							
Power Dissipation		P _{hp}			22.5	W	
Power Supply Current	Instantaneous peak current	I _{CC,ip,hp}			9.0	A	
	Sustained peak current	I _{CC,sp,hp}			7.5		
	Steady state current	I _{CC,hp}			7.2		
Low Speed I/O							
Output Voltage, SCL and SDA	Output low	V _{OL}	0.0		0.4	V	
	Output high	V _{OH}	V _{CC} - 0.5		V _{CC} + 0.3		
Input Voltage, SCL and SDA	Input low	V _{IL}	-0.3		0.3×V _{CC}	V	
	Input high	V _{IH}	0.7×V _{CC}		V _{CC} +0.5		
Capacitance for SCL and SDA I/O signal		C _i			14	pF	
Total Bus Capacitive Load for SCL and SDA	400kHz clock rate, 3.0kΩ pull-up, max.	C _b	100			pF	1
	400kHz clock rate, 1.6kΩ pull-up, max.				200		

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Input voltage / current, InitMode, ResetL and ModSelL	Input voltage, low	V_{IL}	-0.3		0.8	V	
	Input voltage, high	V_{IH}	2.0		$V_{CC}+0.3$		
	Input current, $0V < V_{in} < V_{CC}$	$ I_{in} $			360	μA	
Output voltage, Intl	Output low, $I_{OL} = 2mA$	V_{OL}	0.0		0.4	V	
	Output high, 10k Ω pull-up resistor to host V_{CC}	V_{OH}	$V_{CC}-0.5$		$V_{CC}+0.3$		
Output voltage, ModPrsL	Output low, $I_{OL} = 2mA$	V_{OL}	0.0		0.4	V	2
	Output high	V_{OH}					

Notes:

- For 1000kHz clock rate refer to Figure 6 in [4].
- ModPrsL can be implemented as a short-circuit to GND on the module.

B. High Speed Data I/O

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Transmitter (Module Input) – 400GAUI-8, 100GAUI-2							
Signaling Rate Per Lane			Per IEEE Std 802.3 [1], Annex 120E, Table 120E-7			GBd	
Differential pk-pk Input Voltage Tolerance						mV	
Differential Input Return Loss						dB	
Differential to Common Mode Input Return Loss						dB	
Differential Termination Mismatch						%	
Module Stressed Input Test							
Single-ended Voltage Tolerance Range						V	
DC Common Mode Voltage						mV	
Receiver (Module Output) – 400GAUI-8, 100GAUI-2							
Signaling Rate Per Lane			Per IEEE Std 802.3 [1], Annex 120E, Table 120E-3			GBd	
AC Common-Mode Output Voltage						mV	

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Receiver (Module Output) – 400GAUI-8, 100GAUI-2							
Differential Peak-to-Peak Output Voltage						mV	
Near-end ESMW						UI	
Near-end Eye Height, Differential						mV	
Far-end ESMW						UI	
Far-end Eye Height, Differential						mV	
Far-end Pre-cursor ISI Ratio					Per IEEE Std 802.3 [1], Annex 120E, Table 120E-3	%	
Differential Output Return Loss						dB	
Common to Differential Mode Conversion Return Loss						dB	
Differential Termination Mismatch						%	
Transition Time						ps	
DC Common Mode Voltage						mV	

V. Digital Diagnostic Functions

The QDD-ZRP-400QQSFP-DD-DCO module supports the diagnostics interface specified in the Mechanical Specification with extensions specified in the OIF Coherent cCMIS implementation agreement. See also Coherent application note AN-2200.

VI.Pin Description

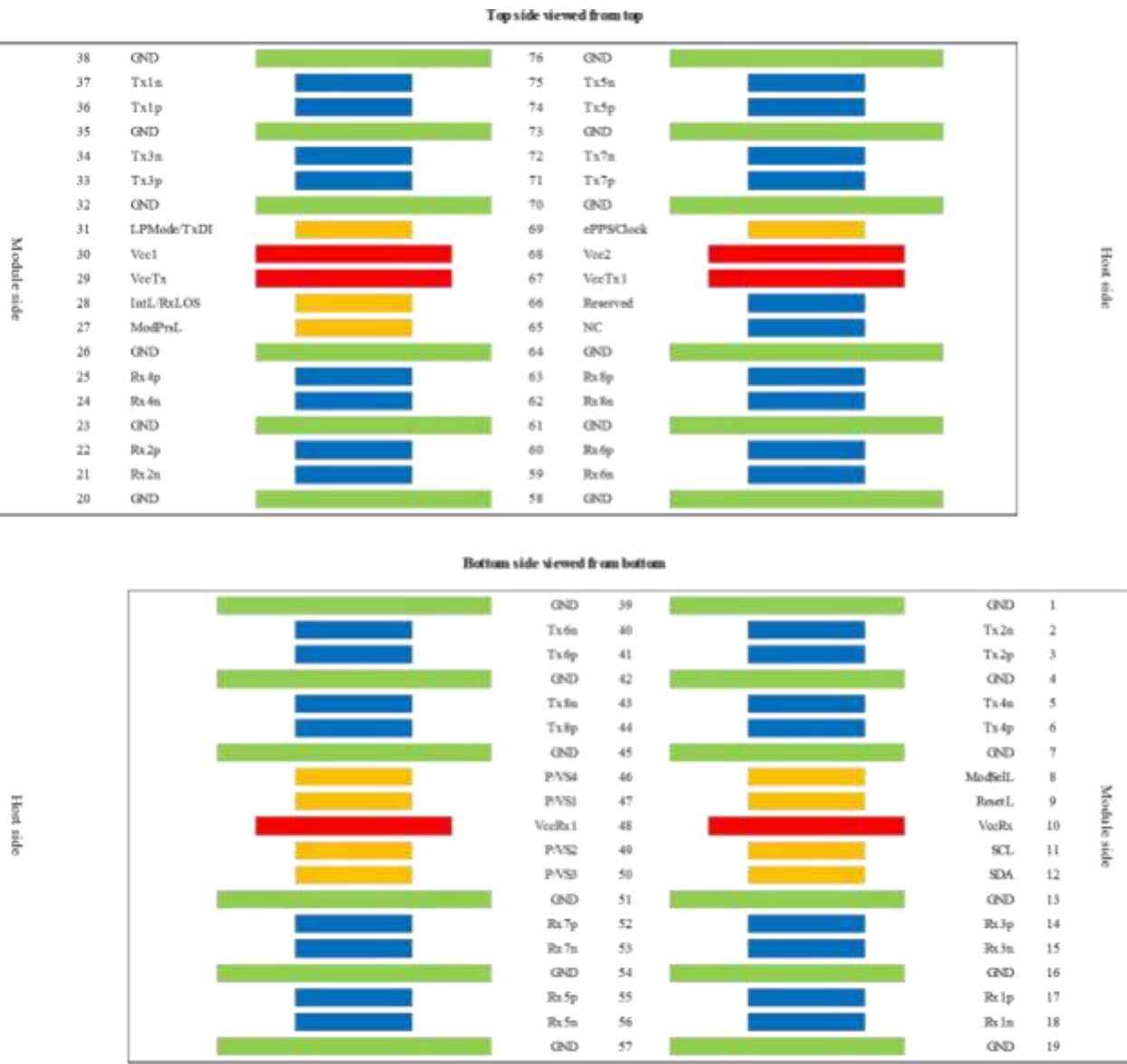


Figure 1 Module Pad Layout

VII. Pin Function Definitions

Pin	Logic	Symbol	Description	Plug Sequence ³	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter inverted data input	3B	
3	CML-I	Tx2p	Transmitter non-inverted data input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter inverted data input	3B	
6	CML-I	Tx4p	Transmitter non-inverted data input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module select	3B	
9	LVTTL-I	ResetL	Module reset	3B	
10		VccRx	+3.3V power supply receiver	2B	2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver non-inverted data output	3B	
15	CML-O	Rx3n	Receiver inverted data output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver non-inverted data output	3B	
18	CML-O	Rx1n	Receiver inverted data output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver inverted data output	3B	
22	CML-O	Rx2p	Receiver non-inverted data output	3B	
23		GND	Ground	1B	1

Pin	Logic	Symbol	Description	Plug Sequence ³	Notes
24	CML-O	Rx4n	Receiver inverted data output	3B	
25	CML-O	Rx4p	Receiver non-inverted data output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module present	3B	1
28	LVTTL-O	IntL/RxLOSL	Interrupt / Optional RxLOS	3B	
29		VccTx	+3.3V power supply transmitter	2B	2
30		Vcc1	+3.3V power supply	2B	2
31	LVTTL-I	LPMode/TxDIS	Low power mode/Optional Tx disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter non-inverted data input	3B	
34	CML-I	Tx3n	Transmitter inverted data input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter non-inverted data input	3B	
37	CML-I	Tx1n	Transmitter inverted data input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter inverted data input	3A	
41	CML-I	Tx6p	Transmitter non-inverted data input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter inverted data input	3A	
44	CML-I	Tx8p	Transmitter non-inverted data input	3A	
45		GND	Ground	1A	1
46	LVC MOS/CML-I	P/V S4	Programmable/Module vendor specific 4	3A	5

Pin	Logic	Symbol	Description	Plug Sequence ³	Notes
47	LVC MOS/CML-I	PVS1	Programmable/Module vendor specific 1	3A	5
48		VccRx1	+3.3V power supply	2A	2
49	LVC MOS/CML-O	PVS2	Programmable/Module vendor specific 2	3A	5
50	LVC MOS/CML-O	PVS3	Programmable/Module vendor specific 3	3A	5
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver non-inverted data output	3A	
53	CML-O	Rx7n	Receiver inverted data output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver non-inverted data output	3A	
56	CML-O	Rx5n	Receiver inverted data output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver inverted data output	3A	
60	CML-O	Rx6p	Receiver non-inverted data output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver inverted data output	3A	
63	CML-O	Rx8p	Receiver non-inverted data output	3A	
64		GND	Ground	1A	1
65		NC	No connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	+3.3V power supply	2A	2
68		Vcc2	+3.3V power supply	2A	2
69	LVC MOS-I	ePPS/Clock	1PPS PTP clock or reference clock input	3A	6

Pin	Logic	Symbol	Description	Plug Sequence ³	Notes
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter non-inverted data input	3A	
72	CML-I	Tx7n	Transmitter inverted data input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter non-inverted data input	3A	
75	CML-I	Tx5n	Transmitter inverted data input	3A	
76		GND	Ground	1A	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector GND contact is rated for a maximum current of 500 mA.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Each connector Vcc contact is rated for a maximum current of 1500 mA.
3. Reserved and No Connect pads recommended to be terminated with 10 k Ω to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.
5. On new designs not used P/V_{Sx} signals are recommended to be terminated on the host with 10 k Ω .
6. ePPS/Clock if not used recommended to be terminated with 50 Ω to ground on the host.

VIII. Optical Characteristics

A. General

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Symbol Rate		Rbaud	30.07		60.14	GBd	
Modulation Format			16QAM, 8QAM, QPSK				
Channel Frequency Range		vC	191.300		196.100	THz	
Channel Spacing	Flexible grid	ΔvC	6.25	100		GHz	
Frequency Accuracy		δvC	-1.5		1.5	GHz	
Frequency Fine Tune Range	Fine tuning with Tx output enabled (bright tuning)	V_{adj}	-6.25		6.25	GHz	
Frequency Fine Tune Resolution					0.10	GHz	
Laser Intrinsic Linewidth	Calculated based on FM noise power spectral density (PSD) measurement	LW			300	kHz	
Side-mode Suppression Ratio	No modulation	SMSR	40			dB	
IRelative Intensity Noise	Peak over 0.2GHz < f < 10GHz	RIN			-140	dB/Hz	
	Average over 0.2GHz < f < 10GHz				-145		

B. Transmitter

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Tx Output Power Configurable Range		$P_{Tx,out}$	-13	0	-7	dBm	1
Tx Output Power Adjustment Resolution					0.1	dB	
Tx Output Power Tolerance		$\delta P_{Tx,out}$	-1.0		1.0	dB	2
Tx Output Power Monitor Range		$P_{Tx,m}$	-14		-6	dBm	
Tx Output Power Monitor Accuracy		$\delta P_{Tx,m}$	-1.0		1.0	dB	3
Tx Output Power During Tuning or When Tx Disabled		$P_{Tx,dark}$			-40	dBm	
Tx Output Power Imbalance Between X- and Y-polarizations		$\Delta P_{X/Y}$			1.0	dB	

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Tx XY Skew					5.0	ps	
Tx IQ Offset					-26	dB	
Tx IQ Imbalance					0.8	dB	
Tx Quadrature Error			-5.0		5.0	°	
Tx IQ Skew					0.75	ps	
Tx In-band Optical Signal to Noise Ratio	Under modulation, $ \Delta f < 150$ GHz	OSNR _{in}	39			dB/0.1nm	
Tx Out-of-band Optical Signal to Noise Ratio	Under modulation, $ \Delta f > 150$ GHz	OSNR _{out}	30			dB/0.1nm	
Tx Reflectance					-27	dB	

- Note:
- 1. Range of target Tx output power values for which other Tx specifications can be maintained.
 - 2. Deviation from target value under closed loop control, over all operating conditions and life.
 - 3. Tx optical output power monitor reading relative to actual Tx output power.

C. Receiver

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Rx Total Input Power		$P_{Rx,tot}$	-30		13	dBm	
Rx Signal Input Power (amplified)	Full Rx OSNR tolerance		-12		0	dBm	1
	Extended range	ZRx00-OFEC	-18		3		
		400ZR	-15		3		
Rx OSNR Tolerance		ZR400-OFEC-16QAM	23.5			dB/0.1nm	
		ZR300-OFEC-8QAM	20.0				
		ZR200-OFEC-QPSK	15.0				
		ZR100-OFEC-QPSK	12.0				
		400ZR	26.0				

Parameter	Conditions		Symbol	Min	Typ	Max	Unit	Notes
CD Tolerance	OSNR penalty < 0.5dB	ZR400-OFEC-16QAM				12.0	ns/nm	2
		ZR300-OFEC-8QAM				18.0		
		ZR200-OFEC-QPSK				24.0		
		ZR100-OFEC-QPSK				48.0		
		400ZR		-2.4		2.4		
PMD Tolerance	OSNR penalty < 0.5dB	ZR400-OFEC-16QAM				20	ps	2
		ZR300-OFEC-8QAM				25		
		ZR200-OFEC-QPSK				25		
		ZR100-OFEC-QPSK				30		
		400ZR				10		
Tolerance to Change in SOP	OSNR penalty < 0.5dB	ZR400-OFEC-16QAM				100	krad/s	2
		ZR300-OFEC-8QAM				180		
		ZR200-OFEC-QPSK				300		
		ZR100-OFEC-QPSK				600		
		400ZR				60		
Polarization Dependent Loss OSNR Penalty	QPSK	1dB PDL				0.3	dB	2
		2dB PDL				0.5		
		4dB PDL				1.5		
	8QAM, 16QAM	1dB PDL				0.5		
		2dB PDL				1.0		
		4dB PDL				2.0		
Rx Signal Input Power Transient Amplitude	Peak excursion from steady state (within Rx signal input power range)			-7		7	dB	
Rx Signal Input Power Transient Rise/Fall Time				0.1			ms	
Rx Signal Input Power (unamplified)	OSNR > 35dB/0.1nm	ZR400-OFEC-16QAM		-23		0	dBm	
		ZR300-OFEC-8QAM		-26		0		
		ZR200-OFEC-QPSK		-30		0		
		ZR100-OFEC-QPSK		-32		0		
		400ZR		-20		0		

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Rx Signal Input Power Monitor Range		$P_{Rx,m(s)}$	-22		1	dBm	
Rx Signal Input Power Monitor Accuracy		$\delta P_{Rx,m(s)}$	-2.0		2.0	dB	
Rx Total Input Power Monitor Range		$P_{Rx,m(t)}$	-22		13	dBm	
Rx Total Input Power Monitor Accuracy	-22dBm to -18dBm	$\delta P_{Rx,m(t)}$	-2.0		2.0	dB	
	-18dBm to +3dBm		-1.5		1.5		
	+3dBm to +13dBm		-2.0		2.0		
Rx Reflectance					-27	dB	

Note:

- 1. Rx signal input power range over which performance can be guaranteed with <1dB OSNR penalty relative to Rx OSNR tolerance limit.
- 2. Rx OSNR penalty is specified for Rx signal input powers < 0dBm.

IX. Module Management Timing Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Optical							
Tx Turn on Time	Warm start				100	ms	
	Cold start				150	s	
Rx Acquisition Time	Warm start				30	ms	
	Cold start				150	s	
Tx/Rx Channel Tuning Time					30	s	
Soft Control and Status Functions							
MgmtInit Duration	Time from power on ₁ , hot plug or rising edge of reset until completion of the MgmtInit State				2000	ms	1
ResetL Assert Time	Minimum pulse time on the ResetL signal to initiate a module reset.		10			μs	
IntL/RxLOS Mode Change Time	Time to change between IntL and RxLOS _L modes of the dual-mode signal IntL/RxLOS _L .				100	ms	

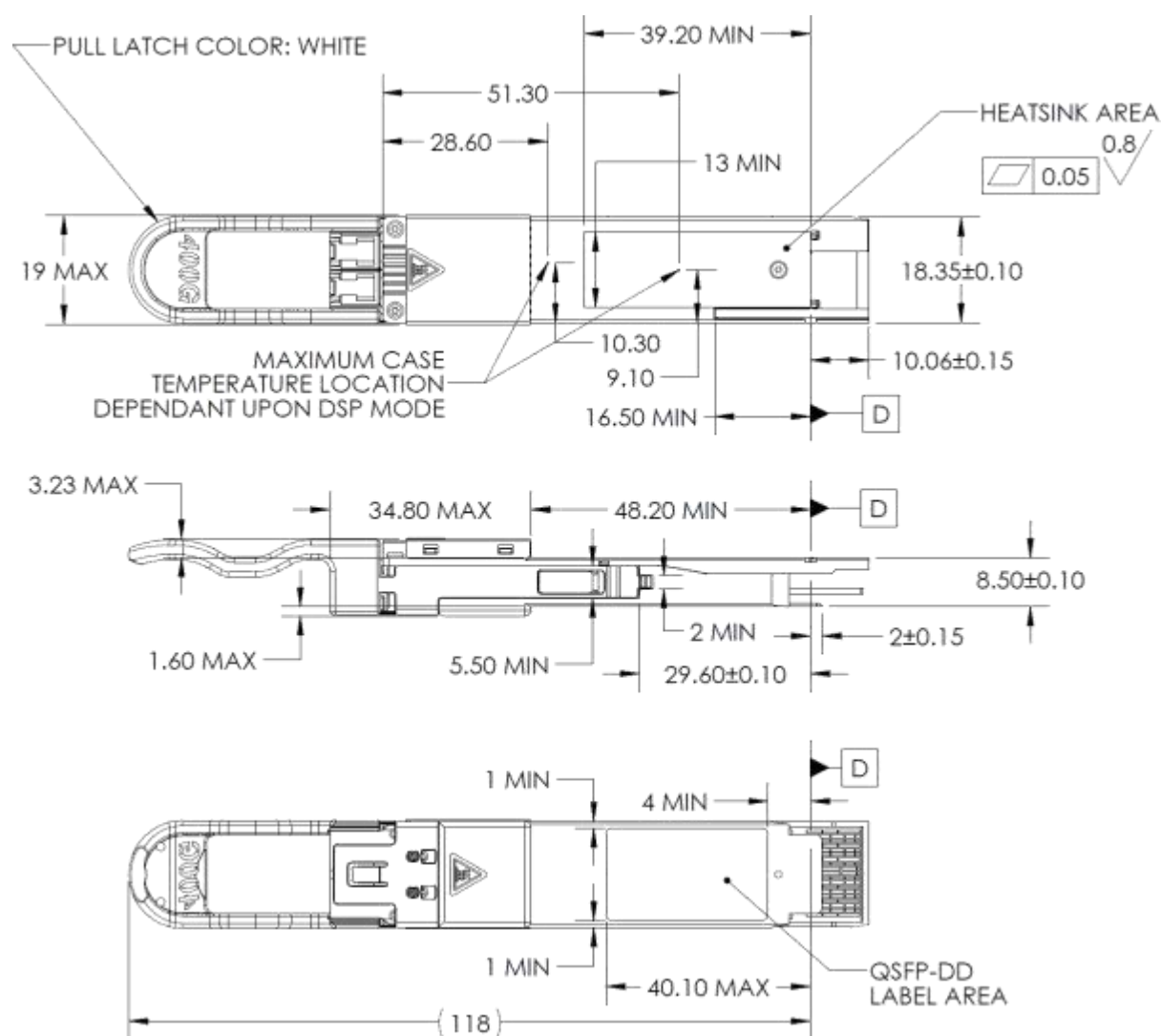
Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Soft Control and Status Functions							
LPMode/TxDis Mode Change Time	Time to change between LPMode and TxDis modes of the LPMode/TxDis signal.				100	ms	
IntL Assert Time	Time from occurrence of condition triggering IntL until Vout:IntL=Vol				200	ms	
IntL Deassert Time	Time from clear on read ² operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.				500	μs	2
RxLOS Assert Time	Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted ³ .				1	ms	3
RxLOS Deassert Time	Time from optical signal above the LOS deassert threshold to when the module releases the RxLOS signal to high.				15	ms	
Tx Disable Assert Time	Time from Tx Disable bit set (value = 1b) ⁴ until optical output falls below 10% of nominal				1	ms	4
Tx Disable Deassert Time	Time from Tx Disable bit cleared (value = 0b) ⁴ until optical output rises above 90% of nominal				100	ms	4
Tx Fault Assert Time	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.				200	ms	
Flag Assert Time	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.				200	ms	
Mask Assert Time	Time from mask bit set (value=1b) ⁵ until associated IntL assertion is inhibited.				100	ms	5
Mask Deassert Time	Time from mask bit cleared (value=0b) ⁵ until associated IntL operation resumes.				100	ms	5
Data Path Tx Turn On Max Duration⁶	Maximum duration of Tx Turn On state.			see CMIS memory 01h:168			6
Data Path Tx Turn Off Max Duration⁶	Maximum duration of Tx Turn Off state.			see CMIS memory 01h:168			6
Data Path Deinit Max Duration⁶	Maximum duration of Data Path Deinit state.			see CMIS memory 01h:144			6
Data Path Init Max Duration⁶	Maximum duration of Data Path Init state.			see CMIS memory 01h:144			6
Module Pwr Up Max Duration⁷	Maximum duration of Module Pwr Up state.			see CMIS memory 01h:167			7
Module Pwr Dn Max Duration⁷	Maximum duration of Module Pwr Dn state.			see CMIS memory 01h:167			7

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
I/O Timing for Squelch & Disable							
Rx Squelch Assert Time	Time from loss of Rx input signal until the squelched output condition is reached.				15	ms	
Rx Squelch Deassert Time	Time from resumption of Rx input signals until normal Rx output condition is reached.				50	ms	
Tx Squelch Assert Time	Time from loss of Tx input signal until the squelched output condition is reached.				400	ms	
Tx Squelch Deassert Time	Time from resumption of Tx input signal until the normal Tx output condition is reached.				1.5	s	
Rx Output Disable Assert Time	Time from Rx Output Disable bit set (value= 1b) ⁴ until Rx output falls below 10% of nominal				100	ms	4
Rx Output Disable Deassert Time	Time from Rx Output Disable bit cleared (value = 0b) ⁴ until Rx output rises above 90% of nominal				100	ms	4
Squelch Disable Assert Time	This applies to Rx and Tx Squelch and is the time from bit set (value = 1b) ⁴ until squelch functionality is disabled.				100	ms	4
Squelch Disable Deassert Time	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b) ⁴ until squelch functionality is enabled.				100	ms	4

Note:

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified.
2. Measured from low to high SDA edge of the Stop condition of the read transaction.
3. RxLOS condition is defined as (a) Rx input power below threshold or (b) DSP loss of signal.
4. Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction.
5. Measured from low to high SDA edge of the Stop condition of the write transaction.
6. Measured from the low to high SDA edge of the Stop condition of the Write transaction until the IntL for the state change Vout:IntL=Vol, unless the module advertises a less than 1 ms duration in which case there is no defined measurement.
7. Measured from the low to high SDA edge of the Stop condition of the Write transaction until the IntL for the state change Vout:IntL=Vol.

X. Mechanical Specifications



Test Center

I. Compatibility Testing

Each fiber optical transceiver has been tested in host device on site in FS Assured Program to ensure full compatibility with over 200 vendors.



Cisco Nexus9000 C 9316D-GX



Arista-DCS-7280DR3 K-24-F



Juniper PTX 10001-36MR



Juniper QFX 5220-32cd



Dell Z9332F-ON



FS N9510-64D

Above is part of our test bed network equipment. For more information, please click the Test Bed PDF. It will be updated in realtime as we expand our portfolio.

II. Test Assured Program

FS.COM truly understands the value of compatibility and interoperability to each optics. Every module FS.COM provides must run through programming and an extensive series of platform diagnostic tests to prove its performance and compatibility. In our test center, we care of every detail from staff to facilities-professionally trained staff, advanced test facilities and comprehensive original-brand switches, to ensure our customers to receive the optics with superior quality.



Our smart data system allows effective product management and quality control according to the unique serial number, properly tracing the order, shipment and every part.



Our in-house coding facility programs all of our parts to standard OEM specs for compatibility on all major vendors and systems such as Cisco, Juniper, Brocade, HP, Dell, Arista and so on.



With a comprehensive line of original-brand switches, we can recreate an environment and test each optics in practical application to ensure quality and distance.



The last test assured step to ensure our products to be shipped with perfect package.

Ordering Information

Part Number	Description
QDD-ZRP-400G	400G QSFP-DD DCO DWDM Tunable Coherent 120km DOM Transceiver